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ABSTRACT

5 A floating gate flash memory device including a substrate including a source region, a drain region and a channel region positioned therebetween; a stack gate including a floating gate electrode, at least one of sidewall/spacers, second sidewalls or a barrier layer, in which the floating gate is positioned above the channel region. The floating gate may be separated from the channel region by one or more of a reverse tunnel dielectric layer, the barrier layer and a pad dielectric layer. The floating gate may be a metal floating gate.